Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-20 (cancelled)

Claim 21 (currently amended): A charge pump circuit for a DRAM comprising:

a first and a second pump cascades coupled in parallel to an output node, each pump cascade having a plurality of pump stages coupled in series, the output node receiving charge pumped by the first and the second pump cascades and providing an output supply voltage that is greater in magnitude than [[the]] a power supply voltage; and

each pump stage having a FET configured as a diode and a FET configured as a capacitor, the FETs of the first pump stage of each cascade having a first oxide thickness and the FETs of the last pump stage of each cascade having a second oxide thickness, the second oxide thickness being greater than the first oxide thickness.

Claim 22 (previously presented): The charge pump circuit of claim 21, wherein (2n)th pump stage of the first pump cascade is coupled to receive a first clock signal and (2n+1)th pump stage of the first pump cascade is coupled to receive a second clock signal, n being an integer greater than or equal to zero;

wherein (2n)th pump stage of the second pump cascade is coupled to receive the second clock signal and (2n +1)th pump stage of the second pump cascade is coupled to receive the first clock signal, n being an integer greater than or equal to zero.

Claim 23 (previously presented): The charge pump circuit of claim 21, where the FETs are PFETs.

Claim 24 (currently amended): The charge pump circuit of claim 21, where the first pump stage of each cascade is coupled to [[a]] the power supply voltage.

Claim 25 (previously presented): The charge pump circuit of claim 21, where each cascade is coupled to the output node by a coupling diode.

Claim 26 (currently amended): The charge pump circuit of claim 25, where the coupling diode is a diode connected FET having a gate oxide of the second [[gate]] oxide thickness.

Claim 27 (previously presented): The charge pump circuit of claim 22, where the first and second clock signals are non-overlapping.

Claim 28 (currently amended): The charge pump of claim 22, where the first and second clock signals are generated from a system clock signal and the charge pump stages pump charge to the

output node in response to both a [[the]] rising edge and a [[the]] falling edge of the system clock signal.

Claim 29 (previously presented): The charge pump circuit of claim 27, where the first and second clock signals are generated from a non overlapping clock signal generator comprising:

a system clock input node;

a clock input stage;

a latch coupled to the clock input stage having intermediate latch outputs and complementary latch outputs;

clock output driving stages coupled to the complementary latch outputs and having non overlapping clock signal outputs;

equalization stage coupled between the clock output driving stages and receiving as inputs the intermediate latch outputs.

Claim 30 (currently amended): A charge pump cascade for use in a DRAM comprising a plurality of pump stages coupled in series with each pump stage having a FET configured as a diode and a FET configured as a capacitor;

the FETs of the first pump stage ~~of each cascade~~ having a first oxide thickness and the FETs of the last pump stage ~~of each cascade~~ having a second oxide thickness where the second oxide thickness is greater than the first oxide thickness;

the first pump stage coupled to a power supply voltage; and

an [[the]] output node receiving charge pumped by the cascade and providing an output supply voltage that is greater in magnitude than the power supply voltage.

Claim 31 (previously presented): The charge pump cascade of claim 30, wherein (2n)th pump stage of the pump cascade is coupled to receive a first clock signal and (2n+1)th pump stage of the pump cascade is coupled to receive a second clock signal, n being an integer greater than or equal to zero.

Claim 32 (previously presented): The charge pump circuit of claim 30, where the FETs are PFETs.

Claim 33 (currently amended): The charge pump cascade of claim 30, where the cascade is coupled to the output node by a diode connected FET having a gate oxide of the second [[gate]] oxide thickness.

Claim 34 (previously presented): The charge pump circuit of claim 31, where the first and second clock signals are non-overlapping.

Claim 35 (previously presented): A method for providing a charge pump circuit for a DRAM comprising the steps of:

coupling first and second pump cascades in parallel to an output node, each pump cascade having a plurality of pump stages coupled in series;

receiving at said output node charge pumped by the first and the second pump cascades to generate a supply voltage thereat that is greater in magnitude than a power supply voltage; and

constructing each pump stage from a FET configured as a diode and a FET configured as a capacitor, the FETs of the first pump stage of each cascade having a first oxide thickness and the FETs of the last pump stage of each cascade having a second oxide thickness, the second oxide thickness being greater than the first oxide thickness.